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Improved transient response using high-frequency feedback control circuit of the constant current ripple constant on-time with native adaptive voltage positioning design for voltage regulators

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Abstract: Improved transient response using high-frequency feedback control (HFFC) circuit of the constant current ripple constant on-time (CCRCOT) with native adaptive voltage positioning design for voltage regulators (VRs) is proposed in this study. The concept uses the HFFC circuit to filter V_{out} at the load transient to change the on-time width dynamically, preventing V_{out} from dropping markedly. This proposal does not need an extra pin to achieve a quick response circuit. Finally, the multiphase VR with the HFFC circuit of the CCRCOT for the IC circuit of the proposed buck converter is implemented by experiment and simulation results to verify their viability and superiority.

1 Introduction

In recent years, over one billion transistors have been integrated in one processor, core static current has been increased from 20 to 100 A, and core voltage has been reduced from 2 to 0.8 V [1–3]. The multiphase voltage regulator (VR) has widely implemented power supply for central processing unit (CPU) application [4–12]. When comparing the multiphase VRs and single-phase VR, the multiphase VRs has a major advantage in the current sharing for each phase and it also reduces power stress of components, like power MOSFET. As such, each phase needs to have a minimum individual off-time limit. The interleaved control also reduces output voltage ripple effectively.

Adaptive voltage positioning (AVP) control scheme has been widely used in multiphase VRs for satisfying the power requirement of Intel's CPUs [3, 13–21]. The basic idea can control output voltage level in the entire voltage tolerance window to be used for the voltage jump or drop during the transient period. The AVP design is a suitable solution to reduce the number of output capacitors, hence reducing VR cost and size.

Recent CPU developments have enhanced power loss reduction when the CPU is on standby. To improve power loss, it is must reduce switching loss and conduction loss when the load is light. A conventional pulse-width-modulation control scheme still has a fixed frequency, which results in a large switching loss. The converter can no longer achieve low loss. The control scheme of the conventional constant on-time (COT) of VRs can reduce switching loss and then increase light load efficiency [22–35] because the switching frequency depends on the loading condition. If the load is light, the switching frequency is reduced to increase efficiency. On the other hand, the pulse skipping modulation (PSM) [36–41] can be combined with the COT to increase light load efficiency because the PSM function turns off the lower-side switch when the inductor current is equal to 0 A. It not only reduces switching loss, but also saves system conduction loss.

However, CPU load transient may occur within 1 μs. COT control is also needed to add a non-linear open-loop quick response circuit to improve transient response. Further, most COT controls provide voltage to CPUs, try to solve this issue by setting up droop-voltage thresholds to trigger another open-loop regulation mechanism, such as triggering another on-time generator or increasing the duty of its on-time generator. However, this kind of design has two major drawbacks. First, the threshold is discrete, which means it may improve transient response over a specific threshold. Second, the threshold is fixed, which cannot meet the verity of loading conditions. Moreover, if the threshold can be set by external components, it suffers another drawback, extra pins, which increase cost and reduce the flexibility of board design.

Our desire is to provide a method, which can maintain a switching regulator's loop stability and characteristic, and also provide a nearly real-time boost response to help the

regulator trace back the correct voltage. This method can allow the droop of output voltage to decide dynamically how fast or what quantity to boost the regulator without the extra setting of pins and to provide board designers the flexibility to change boost speed.

2 Native AVP design for VRs

Fig. 1 shows the native AVP (NAVP) design of the constant current ripple COT (CCRCOT) for VRs [4]. This control scheme not only has CCRCOT [42], but also the ability to cancel the steady-state error. The EA is an error amplifier and the V_{comp1} signal is the output of error amplifier. Two input signals of error amplifier are the feedback signal V_{fb} and the voltage identification definition (VID) voltage, so the output voltage has changed by the VID voltage. S11, S12 and S13 are the upper-side switches, S21, S22 and S23 are the lower-side switches, L_1, L_2 and L_3 is the output inductor and R_{CO} is the equivalent series resistance of the output capacitor C_O. The current source I_{LOAD} is the output load. The trigger signal V_{trig} is the output of comparator to drive on-time generator.

Fig. 2 shows the steady-state error cancelled of the native AVP design. A near-DC voltage is added between the output of the error amplifier, V_{comp1} and the positive input of the comparator. The V_{comp2} can make the V_{comp1} voltage higher in steady-state and hence low the V_{out} back to its expected value. The V_{comp_ofs} voltage is a droop between the V_{comp1} voltage and the V_{comp2} voltage. The DC voltage is generated by a low-pass filter (LPF) subtraction of the V_{cs} and V_{comp2} ripple voltages which are in front of the comparator. The frequency of LPF should be designed much smaller than the switching frequency.

Refer to the steady-state control signals at the 'A' point shown in Fig. 2 to obtain (1)–(3)

$$V_{cs,Vally} = V_{comp2,Peak} \tag{1}$$

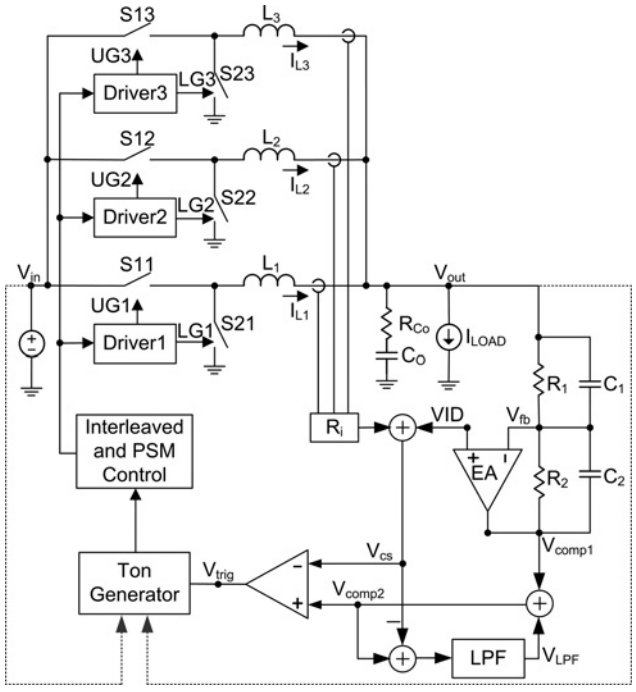

Fig. 1 *Native AVP design of the CCRCOT for VRs*

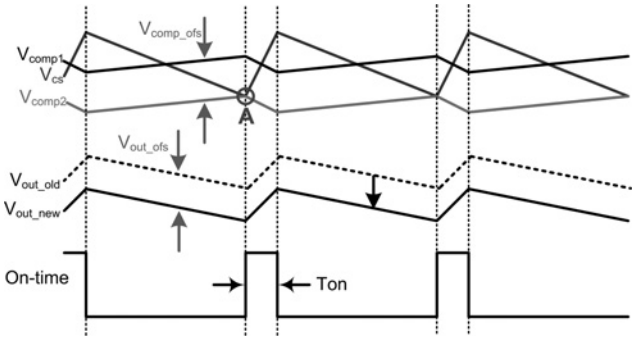

Fig. 2 *Steady-state error cancelled of the NAVP design*

$$\mathrm{VID} + \left(R_i\left(I_L - \frac{\Delta I_L}{2}\right)\right) = V_{comp1} + V_{LPF} \tag{2}$$

$$\begin{aligned}\mathrm{VID} + \left(R_i\left(I_L - \frac{\Delta I_L}{2}\right)\right) &= \mathrm{VID} \\ &+ A_V\left(\mathrm{VID} - \left(V_{out} - \frac{\Delta V_{out}}{2}\right)\right) + V_{LPF}\end{aligned} \tag{3}$$

$$V_{LPF} = -A_V\frac{\Delta V_{out}}{2} - R_i\frac{\Delta I_L}{2} \tag{4}$$

V_{LPF} is described in (4) and, by substituting (4) for (3), (5)–(7) can be obtained

$$V_{out} = \mathrm{VID} - \frac{R_i}{A_V}I_L \tag{5}$$

$$R_{DROOP} = \frac{R_i}{A_V} \tag{6}$$

$$A_V = \frac{R_2}{R_1} \tag{7}$$

A_V is the desired error amplifier gain. R_i is the internal current sense amplifier gain. R_{DROOP} is the current sense resistor. This control also implements the AVP function easily. R_{DROOP} should be designed to determine the load line. It is the equivalent load line resistance as well as the desired static output impedance.

An optimised compensation of a multiphase VR allows for the best possible load step response of its output. A type-II compensator with one pole and one zero is adequate for proper compensation. A prior design procedure shows how to decide the resistive feedback components of an error amplifier gain. C_1 and C_2 must be calculated for compensation by (8). The target is to achieve constant resistive output impedance over the widest possible frequency range

$$G_{VC}(s) = \frac{R_i}{R_{DROOP}}\frac{1 + s/R_1\,C_1}{1 + s/R_2\,C_2} \tag{8}$$

Fig. 3 shows the on-time generator circuit of the CCRCOT, which samples the input voltage and the VID voltage to determine the width of the on-time. The 'TON' is a pin of the IC through a resistor connected to the input voltage of V_{in}. It also samples the VID voltage by (9). The voltage drop between input voltage and VID voltage depends on the inductor current ripple by (10). Therefore, even if the

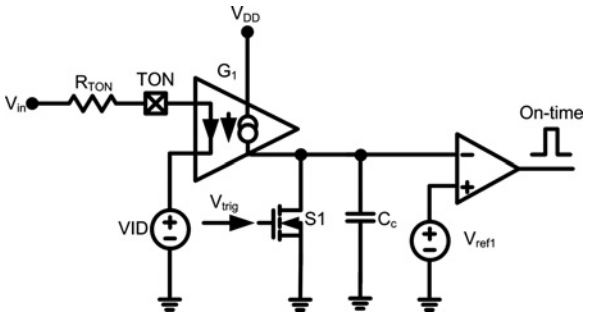

Fig. 3 *On-time generator circuit of the CCRCOT*

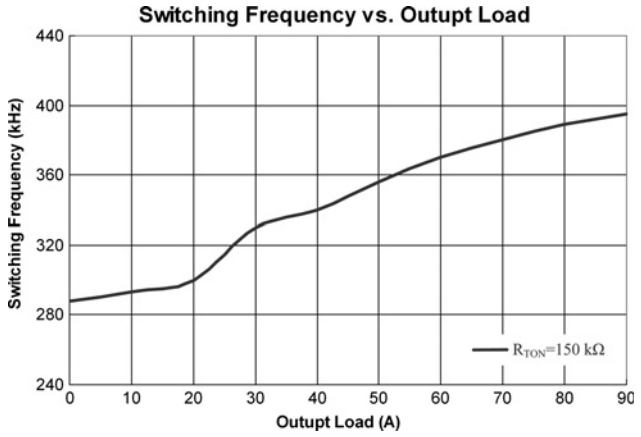

Fig. 4 *Experimental results for the switching frequency against the output load of the CCRCOT*

voltage drop is changed, the inductor current ripple maintains a constant value. Hence, CCRCOT is suitable for different input and VID voltages to obtain the same output voltage ripple, such as CPU applications

$$T_{\mathrm{ON}} = \frac{R_{\mathrm{TON}}}{V_{\mathrm{in}} - \mathrm{VID}} \times C_c \times V_{\mathrm{ref1}} \tag{9}$$

$$T_{\mathrm{ON}} = \frac{L}{V_{\mathrm{in}} - V_{\mathrm{out}}} \times \Delta I_L \tag{10}$$

When the resistor of R_{TON} is changed, the width of on-time is also changed. Switching frequency depends on the voltage drop between the input and the output voltages. Fig. 4 shows the experimental results for the switching frequency against the output load of the CCRCOT ($V_{\mathrm{in}} = 12$ V, VID = 0.7 V). Experimental results show that at an output load of 0–90 A, when the resistor of R_{TON} is 150 kΩ, the switching frequency increases from 288 to 395 kHz.

Fig. 5 shows the experimental results for the output voltage ripple against the output load of the CCRCOT ($V_{\mathrm{in}} = 12$ V, VID = 0.7 V). Experimental results show the operation at an output load of 0–90 A. The inductor current ripple maintains a consistent value to obtain the same output voltage ripple, such as 8 mV.

Fig. 6 shows the experimental results for the output voltage ripple of the CCRCOT. The operation conditions are set at 0.7 V output voltage and 90 A output load to measure the output voltage ripple for 12 V input voltage.

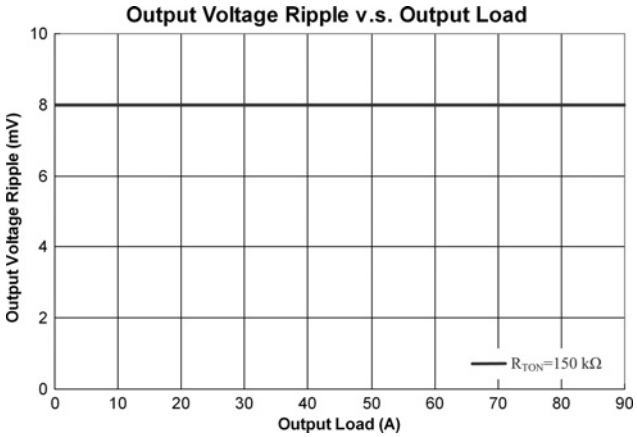

Fig. 5 *Experimental results for the output voltage ripple against the output load of the CCRCOT*

3 Conventional quick response circuit of the CCRCOT with native AVP design for VRs

Recently, two types of improved transient response circuits have been used, namely, the internal fixed quick response circuit by IC design [43, 44], and the external setting by component or voltage source [42]. The internal fixed quick response circuit by IC design usually uses V_{fb} to determine and trigger the quick response function, which can provide longer on-time width to the driver circuit. The main advantage of this process is that no extra pin in the IC is needed to achieve this function. However, the generator circuit of the quick response function is not convenient to use in CPU applications because it cannot be designed to control the on-time width during different load conditions. On the other hand, the hysteresis of the comparator is hard to design, especially for very fast load transient like CPU applications. If the hysteresis of the comparator is too small, it can induce the system to trigger a longer on-time width erroneously, thereby causing a high ripple of V_{out}. Conversely, if the hysteresis of the comparator is too large, it can render the quick response function unavailable.

Fig. 7 shows the external setting quick response circuit of the on-time generator circuit of the CCRCOT. The operational principle of the external setting quick response circuit requires the addition of a voltage source V_{QRSET} to determine the width of QR-time. V_{QRSET} is connected to the

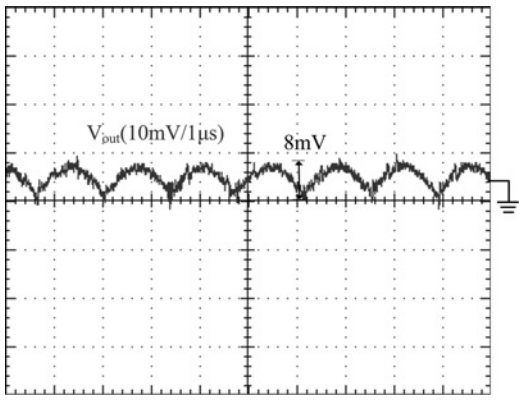

Fig. 6 *Experimental results for the output voltage ripple of the CCRCOT*

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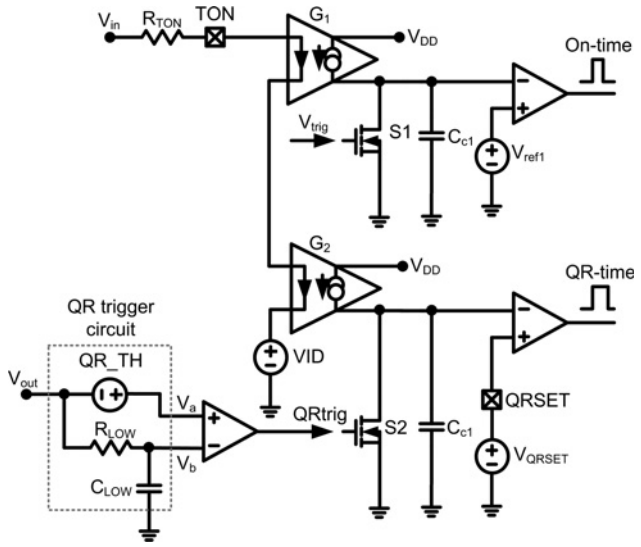

Fig. 7 *External setting quick response circuit of the on-time generator circuit of the CCRCOT*

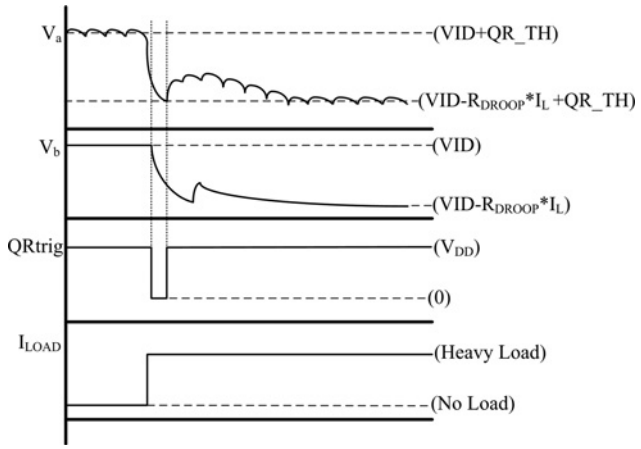

Fig. 8 *Control signals for QR trigger circuit of external setting quick response circuit*

'QRSET' pin. If the QR-time needs a large on-time width, the user should design V_{QRSET} to be larger than or equal V_{ref1}.

The QR trigger circuit samples the V_{out} signal and uses the LPF to cause the V_{out} signal delay and a DC source of QR_TH as shown in Fig. 8. At a steady state, the droop of V_{out} cannot trigger the QR-time. When this abrupt voltage droop is lower than the QR threshold level, the QR trigger circuit generates a low-level signal that turns off the switch of S2 [42]. The frequency of the LPF for R_{LOW} and C_{LOW} should be designed to be much smaller than the switching frequency because the output voltage ripple may cause this system to have a failure in operation with QR-time. The QR_TH signal can be designed in IC or set by the user with the pin [42].

The main advantage of the external setting quick response circuit can depend on the load conditions to design the V_{QRSET} value generating a suitable QR-time in this system. However, this method requires two extra IC pins to achieve the quick response function.

4 Improved transient response using high-frequency feedback control (HFFC) circuit of the CCRCOT with native AVP design for VRs

Improved transient response using HFFC circuit of the CCRCOT with native AVP design for VRs is proposed in this paper as shown in Fig. 9. It is an external setting device that uses these components design, not a voltage source to set up. This HFFC circuit does not require any extra pin to achieve the quick response function of ICs. The system consists of resistor R_q and capacitor C_q in a series that are connected between the V_{out} and the 'TON' pin. It operates under the principle that the high-pass filter filters high-frequency signals to pass from the V_{out} to the 'TON' pin by (11). However, the frequency of the high-pass filter must be larger than or equal the switching frequency so the steady-state operation of the system is not affected. On the other hand, the user may base the design of the resistor R_q and the capacitor C_q on the worst-case operation (maximum load step)

$$F_{\mathrm{RC}} = \frac{1}{2\pi R_q C_q} \geq F_S \tag{11}$$

When light load quickly transforms quickly into a heavy load, V_{out} drops momentarily through the coupling by the capacitor C_q, which allows the resistor R_q to cause a voltage drop. The voltage drop of R_q forms a current of I_2, so the R_q needs to be designed first because the current of I_2 can change the width of on-time directly as shown in Fig. 10. However, a longer width of on-time makes the converter to deliver more energy from the input terminal to the output load. If R_q has changed small, the width of on-time becomes longer. On the other hand, the capacitor of C_q should be designed with the frequency of the high-pass filter. The calculation of the Laplace transform formula is shown by (12)

In the multiphase operation, the HFFC circuit not only increases longer on-time width directly, but also controls the driver in each phase synchronously.

The advantages of this HFFC circuit are the follows:

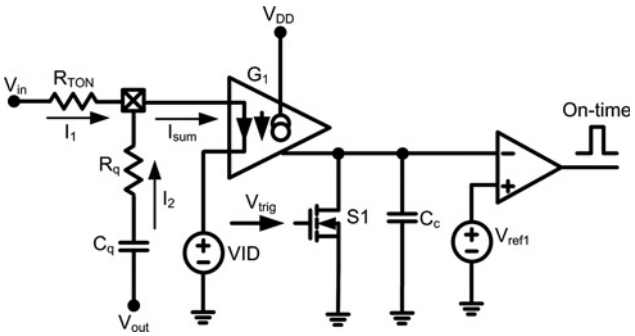

Fig. 9 *HFFC circuit of on-time generator circuit of the CCRCOT*

$$\mathrm{Ton}(s) = \frac{C_c}{G_1\left(\left(V_{\mathrm{in}} - \mathrm{VID}\right)/R_{\mathrm{TON}} + \left(s\,C_q\,V_{\mathrm{out}} - \mathrm{VID}\right)/\left(1 + s\,C_q\,R_q\right)\right)}\,V_{\mathrm{ref1}} \tag{12}$$

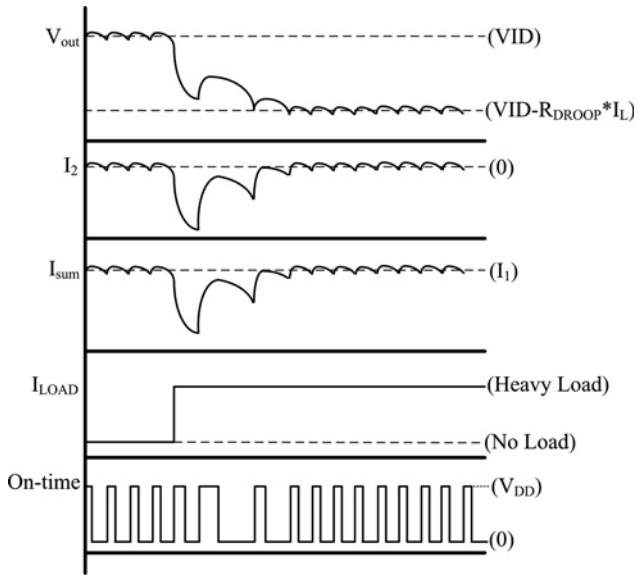

Fig. 10 *Control signals for HFFC circuit of on-time generator circuit of the CCRCOT*

1. It clearly generates a longer width of on-time that is proportional to the output voltage droop.
2. Adaptation to the width of on-time depends on the load conditions of the system.
3. It only uses one generator circuit; thus, it is very convenient to design and to apply.
4. It does not require an extra pin to achieve the quick response function of IC.

5 Experimental verification

To understand the feasibility and the performance of this HFFC circuit of the CCRCOT with native AVP design for VRs, experimental results with multiphase operation are shown to prove that it is viable and useful. The operation conditions are as follows:

1. Input DC voltage (V_{in}): 12 V
2. Output DC voltage (VID): 0.7 V
3. Output load (I_{LOAD}): 35–75 A
4. Switching frequency (F_S): 288–395 kHz
5. Upper-side MOSFET: IPS09N03LA*3
6. Lower-side MOSFET: IPS06N03LA*6
7. Compensation circuit: $R_1 = 10$ kΩ, $R_2 = 47$ kΩ, $C_1 = 80$ pF, $C_2 = 100$ pF
8. Load line (R_{DROOP}): 2.25 mΩ
9. Current sense amplifier gain (R_i): 10
10. Main inductor : 360 nH*3
11. Output capacitors (C_O): $C_{OS-CAP} = 560$ µF/2.5 V (R_{CO}: 7 mΩ)*3, $C_{MLCC-CAP} = 22$ µF/6.3 V (R_{CO}: 3 mΩ)*22
12. HFFC circuit (Fig. 9) : $G_1 = 147.54$ m (A/A); $R_{TON} = 150$ kΩ; $C_c = 3$ pF; $R_q = 330$ Ω; $C_q = 560$ pF; $V_{ref1} = 1.2$ V
13. External setting quick response circuit (Fig. 7): $R_{LOW} = 600$ kΩ; $C_{LOW} = 2$ pF; $G_1 = 147.54$ m (A/A); $R_{TON} = 150$ kΩ; $C_c = 3$ pF; $V_{ref1} = 1.2$ V; $V_{QRSET} = 1.2$ V; QR_TH = 35 mV

Fig. 11 shows the chip layout of the control IC, in which the on-time generator and loop control are both occupied. The area is marked with a die size of 3040 µm × 2300 µm.

Fig. 12 shows a comparison of the experimental results at droop with the HFFC circuit (Fig. 9) and that without quick response circuit (Fig. 3). The blue waveform has no quick response circuit for the output voltage, whereas the red waveform has the HFFC circuit for the output voltage. The output voltage signals are based on the same measured output current load, such as the black waveform, which is used as a voltage transient test (VTT) tool to achieve transient load.

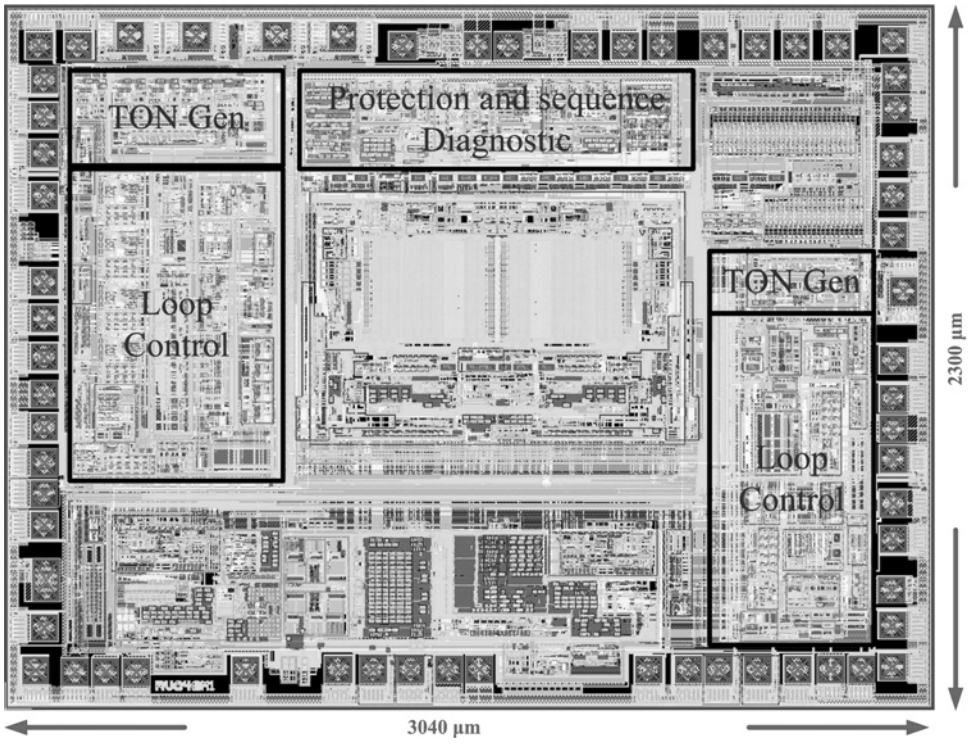

Fig. 11 *Chip layout of the control IC*

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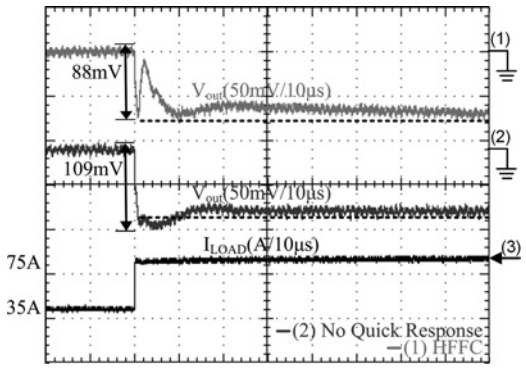

Fig. 12 *Comparison of the experimental results at droop with the HFFC circuit and that without quick response circuit*

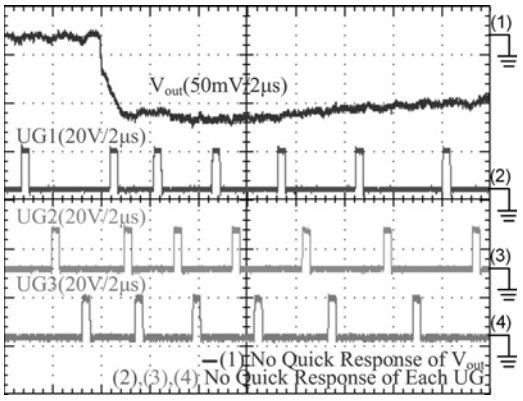

Fig. 13 *Experimental results of the output voltage and control signals at droop without quick response circuit*

V_{out} at the load transient with the HFFC circuit is 88 mV and V_{out} at the load transient without quick response circuit is 109 mV. Hence, V_{out} with the HFFC circuit is not only lower by 11 mV than that without quick response circuit, but also has a lower voltage to meet the load line specification as shown by the black dot line. The load line specification has 90 mV and it is also equal to the R_{DROOP} 2.25 mΩ to multiply the output load step 40 A.

Fig. 13 shows the experimental results of the output voltage and control signals at droop without quick response circuit. The blue waveform is that without quick response circuit for the output voltage, whereas the green waveform is that without quick response circuit for the UG1 signal, whereas the orange waveform is that without quick response circuit for the UG2 signal, whereas the pink waveform is that without quick response circuit for the UG3 signal. These control signals have the same width of on-time and a sequencing control. On the other hand, these control signals cannot drive each phase synchronously to deliver more energy from the input terminal to the output load.

Fig. 14 shows the experimental results of the output voltage and control signals at droop with the HFFC circuit. The red waveform is that with the HFFC circuit for the output voltage signal, whereas the green waveform is that with the HFFC circuit for the UG1 signal, whereas the orange waveform is that with the HFFC circuit for the UG2 signal, whereas the pink waveform is that with the HFFC circuit for the UG3 signal. These control signals with the HFFC circuit are obviously longer than those without quick response during the output load, from light load to heavy

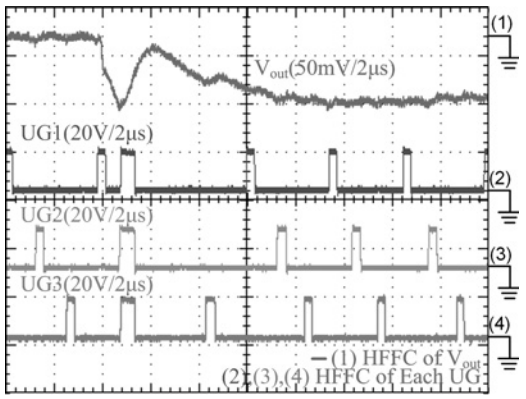

Fig. 14 *Experimental results of the output voltage and control signals at droop with the HFFC circuit*

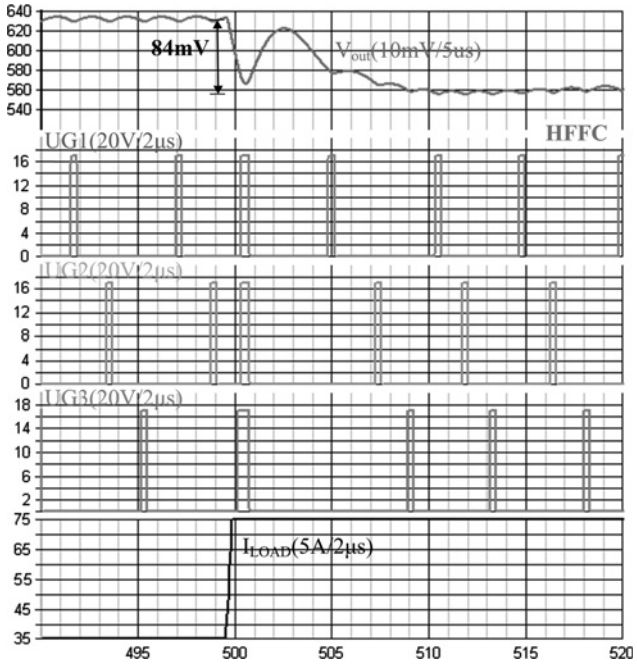

Fig. 15 *Simulation results of the output voltage and control signals at droop with the HFFC circuit*

load. On the other hand, these control signals can drive all phases synchronously to deliver more energy from the input terminal to the output load.

Fig. 15 shows simulation results of the output voltage and control signals at droop with the HFFC circuit. The red waveform is that with the HFFC circuit for the output voltage signal, whereas the green waveform is that with the HFFC circuit for the UG1 signal, whereas the orange waveform is that with the HFFC circuit for the UG2 signal, whereas the pink waveform is that with the HFFC circuit for the UG3 signal. These control signals with the HFFC circuit are obviously longer than those without quick response during the output load, from light load to heavy load. On the other hand, these control signals can drive all phases synchronously to deliver more energy from the input terminal to the output load to prevent the output voltage from dropping markedly. Thus, SIMPLIS simulation and experimental results can be verified each other.

To further understand the advantage and the superiority of this HFFC circuit, this paper plans to base identical operation

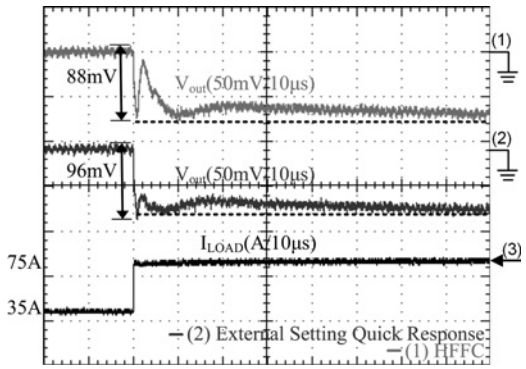

Fig. 16 *Comparison of the experimental results at droop with the HFFC circuit and that external setting quick response circuit*

conditions by comparing the external setting quick response circuit.

Fig. 16 shows a comparison of the experimental results at droop with the HFFC circuit (Fig. 9) and that external setting quick response circuit (Fig. 7). The blue waveform is that with external setting quick response circuit for the output voltage, whereas the red waveform is that with the HFFC circuit for the output voltage. The output voltage signals are based on the same measured output current load, such as the black waveform used as VTT tool to achieve load transient.

V_{out} at droop with the HFFC circuit is 88 mV and V_{out} at droop with external setting quick response circuit is 96 mV. Thus, V_{out} with the HFFC circuit and the external setting quick response circuit are close. The HFFC circuit and the external setting quick response circuit are both useful to prevent the V_{out} from dropping markedly, but the HFFC circuit does not require an extra pin to achieve the quick response function of IC.

6 Conclusions

This paper is proposed improved transient response using HFFC circuit of the CCRCOT with native AVP design for VRs. The concept of this HFFC circuit uses the capacitor and the resistor in a series to filter out the output voltage at load transient to change the width of on-time dynamically to prevent the V_{out} from dropping markedly.

Both experimental and simulation verifications confirm that the proposed the HFFC circuit of the CCRCOT with native AVP design for VRs can significantly improve transient response. Moreover, the proposed HFFC circuit has very simple structure and design. It is available and useful with native AVP design for VRs.

7 Acknowledgment

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